Amendments to the Claims:

This listing of the claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate having two types of active regions that are a PMOS region and an NMOS region separated from each other in plan view by a PN separation film; and

a dual-gate electrode extending linearly across said PMOS region, said PN separation film and said NMOS region collectively on an upper side of said semiconductor substrate,

said dual-gate electrode including a P-type portion positioned on said PMOS region, an N-type portion positioned on said NMOS region and a PN junction positioned between said P-type portion and said N-type portion, and

said PN junction including a silicide region having been subjected to silicidation, and said silicide region is apart from both said PMOS region and said NMOS region and ~~formed~~ confined solely within an area of said PN separation film in plan view.

2 (Original): The semiconductor device according to claim 1, wherein said dual-gate electrode is substantially covered with a silicidation prevention film except for said silicide region.

3 (Original): The semiconductor device according to claim 2, wherein said silicidation prevention film includes a silicon nitride film.

4 (Original): The semiconductor device according to claim 1 further comprising a contact positioned on said active regions such that said contact overlaps said dual-gate electrode in plan view.

5 (Original): The semiconductor device according to claim 4, wherein said contact is positioned to avoid said silicide region in plan view.

6 (Original): The semiconductor device according to claim 4, wherein said contact is positioned to avoid said PN separation film in plan view.

7 (New): A semiconductor device comprising:

a semiconductor substrate having two types of active regions that are a PMOS region and an NMOS region separated from each other in plan view by a PN separation film;

a gate oxide film formed overlying said semiconductor substrate; and

a dual-gate electrode formed overlying said gate oxide film and extending linearly across said PMOS region, said PN separation film and said NMOS region collectively on an upper side of said semiconductor substrate,

said dual-gate electrode including a P-type portion positioned on said PMOS region, an N-type portion positioned on said NMOS region and a PN junction positioned between said P-type portion and said N-type portion, and

said PN junction including a silicide region having been subjected to silicidation, wherein said silicide region is in contact with said gate oxide film, and said silicide region is apart from both said PMOS region and said NMOS region and formed within an area of said PN separation film in plan view.